REMARKS

Claims 1, 3-16, and 18-19 are pending in the present application. Claims 1, 3 and 10-11 were rejected under 35 U.S.C. §102, as anticipated by U.S. Patent Application Publication No. 2002/0042909 (Van Gageldonk, *et al.*), and claims 4-9 and 12-6 and 18-19 were rejected under 35 U.S.C. §103 as obvious over Van Gageldonk in view of U.S. Patent Application Publication No. 2001/0004755 (Levy, *et al.*). Applicant has amended claims 1, 10-12, and 14-15, and has canceled claims 2 and 16. No new matter has been introduced.

Applicant urges that claims 1, 3, 10 and 11 are not anticipated by Van Gageldonk for at least the reasons presented below.

At the very least, Van Gageldonk does not disclose or suggest a microprocessor for processing instructions that includes *a plurality of register sub-files each having a plurality of registers for storing data for executing the instructions, wherein the register sub-files each have a same number of registers,* as essentially recited in claim 1.

The Examiner cites register files RF1 and RF2 in Fig. 1 of Van Gageldonk as disclosing register sub-files having a same number of registers. However, the section of Van Gageldonk that describes the register files, paragraph [0025], discloses nothing regarding the number of registers in each register sub-file. Paragraph [0025] instead describes how the functional units are connected to the register sub-files, and how the physical registers can be organized within the register sub-file. Applicant urges that the Examiner is incorrect in stating that Van Gageldonk discloses register sub-files having a same number of registers. Furthermore, Van Gageldonk's FIG. 1 depicts register sub-files of different sizes connected to functional unit clusters of different sizes, which suggests that Van Gageldonk's register sub-files can have a different number of registers.

Thus, for the reasons presented above, Applicant urges that Van Gageldonk does not anticipate claim 1. Reconsideration and withdrawal of this section 102 rejection are respectfully requested.

Applicant urges that claim 10, as amended, is not anticipated by Van Gageldonk for at least the reasons presented below.

At the very least, Van Gageldonk does not disclose or suggest a system for processing an instruction in a microprocessor wherein *each of the plurality of register files has at least one read port from which any of the plurality of clusters can read data,* as essentially recited in claim 10.

Van Gageldonk's FIG. 1 and its supporting text, paragraphs [0023] and [0025], disclose functional unit clusters and register files where one or more functional unit clusters write to or read from the same register file. Van Gageldonk does not disclose functional unit clusters that can read from any of the register files, as recited in claim 10.

Thus, for the reasons presented above, Applicant urges that Van Gageldonk does not anticipate claim 10. Claim 11 depends from claim 10 and is patentable for at least the same reasons as claim 10. Reconsideration and withdrawal of these section 102 rejections are respectfully requested.

Claims 4-9 depend from claim 1, and claims 12-14 depend from claim 10. The Action cited Levy as disclosing a register-renaming unit as recited in claims 4 and 12. However, although Levy discloses functional units and register files, Levy does not disclose the *register sub-files [that] have a same number of registers*. Thus, Applicant urges that Levy does not correct for the deficiencies of Van Gageldonk. Therefore, Applicant urges that a *prima facie* case of obviousness of claims 4-9 and 12-14 cannot be maintained over Van Gageldonk and Levy. Reconsideration and withdrawal of these rejections are respectfully requested.

Applicant urges that claim 15 is not obvious over Van Gageldonk in view of Levy for at least the reasons presented below.

As stated above, Van Gageldonk does not disclose or suggest a microprocessor or method of processing instructions in a microprocessor that includes *a plurality of register sub-files each having a plurality of registers for storing data for executing the instructions, wherein the register sub-files each have a same number of registers,* as essentially recited in claim 15. The Examiner cited Levy for disclosing renaming target registers in the instruction with registers in a register sub-file. However, although Levy discloses floating point registers and integer registers, Levy does not disclose the *register sub-files each have a same number of registers*, and thus Levy does not rectify the deficiencies of Van Gageldonk.

Thus, Applicant urges that a *prima facie* case of obviousness of claim 15 over Van Gageldonk and Levy cannot be maintained. Reconsideration and withdrawal of this section 103 rejection are respectfully requested.

Claims 18-19 depend from claim 15, and are thus patentable for at least the same reasons as claim 15. Reconsideration and withdrawal of these rejections are respectfully requested.

CONCLUSION

Applicant urges that claims 1, 4-15, and 18-19 are in condition for allowance for at least the reasons stated. Early and favorable action on this case is respectfully requested.

Respectfully submitted,

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